

IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Currently Amended) A power transistor device comprising:
 - 5 a substrate;
 - a device film formed on the substrate; and
 - an adhesion layer formed on a side of the substrate opposite the device film, wherein at least a portion of the adhesion layer is at least partially segmented and configured to be thermally coupled to a heat sink;
 - 10 the power transistor device thereby exhibiting a reduced amount of bowing relative to an amount of bowing expected without the segmenting of the adhesion layer.
2. (Original) The device of claim 1, wherein the adhesion layer comprises a material selected from the group consisting of titanium, nickel and combinations comprising at least one
 - 15 of the foregoing materials.
3. (Original) The device of claim 1, wherein the adhesion layer comprises material arranged in distinct segments, each segment being at least partially separated from other segments of the adhesion layer.
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4. (Original) The device of claim 3, wherein voids between one or more of the segments are substantially free of material.
5. (Original) The device of claim 3, wherein voids between one or more of the
 - 25 segments comprise a low stress material.

6. (Original) The device of claim 5, wherein the low stress material comprises a low stress polymer.
7. (Original) The device of claim 1, wherein the adhesion layer comprises material arranged in distinct segments that are uniformly spaced along the adhesion layer.
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8. (Original) The device of claim 1, wherein the adhesion layer comprises material arranged in distinct segments that are non-uniformly spaced along the adhesion layer.
- 10 9. (Original) The device of claim 1, wherein the adhesion layer comprises one or more voids, at least one of which extends partially through the adhesion layer.
10. (Original) The device of claim 1, wherein the adhesion layer has a thickness of from about 100 angstroms to about 1,000 nanometers.
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11. (Original) The device of claim 1, further comprising at least one additional metal-containing layer associated with a side of the adhesion layer opposite the substrate.
12. (Original) The device of claim 11, wherein one or more of the at least one additional metal-containing layer is segmented.
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13. (Original) The device of claim 1, further comprising a barrier layer associated with a side of the adhesion layer opposite the substrate.
- 25 14. (Original) The device of claim 13, wherein the barrier layer comprises a metal selected from the group consisting of platinum, niobium and combinations comprising at least one of the foregoing metals.

15. (Original) The device of claim 1, further comprising a wettable-surface layer associated with a side of the adhesion layer opposite the substrate.

16. (Original) The device of claim 15, wherein the wettable-surface layer comprises a metal selected from the group consisting of gold, tin, silver, lead, germanium, bismuth, indium and combinations comprising at least one of the foregoing metals.

17. (Currently Amended) A method of processing a power transistor device, the method comprising the steps of:

10 forming a device film on a substrate;
forming an adhesion layer on a side of the substrate opposite the device film; and
at least partially segmenting at least a portion of the adhesion layer and configured to be thermally coupled to a heat sink, the power transistor device thereby exhibiting a reduced amount of bowing relative to an amount of bowing expected without the segmenting
15 of the adhesion layer.

18. (Currently Amended) An integrated circuit, comprising:

20 at least one power transistor device comprising:
a substrate;
a device film formed on the substrate; and
an adhesion layer formed on a side of the substrate opposite the device film, wherein at least a portion of the adhesion layer is at least partially segmented and configured to be thermally coupled to a heat sink;
the power transistor device thereby exhibiting a reduced amount of
25 bowing relative to an amount of bowing expected without the segmenting of the adhesion layer.

19. (Original) The integrated circuit of claim 18, wherein the at least a portion of the adhesion layer is at least partially segmented by patterning along two or more intersecting axes of the power transistor device.

5 20. (Original) The integrated circuit of claim 18, wherein the adhesion layer comprises a material selected from the group consisting of titanium, nickel and combinations comprising at least one of the foregoing materials.